



Leadframe Design Enhancement for Elimination of Burrs at Singulation Process

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

The paper focused on the improvement done in leadframe design to address the copper (Cu) burrs defect in assembly manufacturing. Newly qualified device struggled to hit the target yield due to the said Cu burrs defect. A holistic approach through why-why analysis was performed by the technical cross-functional team to identify the root-cause and come-up with the robust solution to the issue. The paper discussed how the device in focus was made as point of reference in designing a leadframe carrier. Ultimately, the new and enhanced leadframe design successfully eliminated the occurrence of Cu burrs with 100% improvement in the scrappage rate.

Keywords: Singulation; copper burrs; leadframe; QFN.

1. INTRODUCTION

A common direction of semiconductor assembly manufacturing companies is to increase the production yields and maintain high quality while minimizing the wastage and assembly rejections. With new and continuous technology trends and breakthroughs, challenges in assembly

manufacturing are unavoidable [1-3]. In this paper, package copper (Cu) burrs is a common defect frequently encountered during package singulation for the device in focus. Cu burrs defect shown in Fig. 1 is defined as excess metals protruding on the leads which may cause severe damaged during applications. Normally, this is brought about by improper blade cutting

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parameters and easy to fix. However, this phenomenon gives question mark on the heads of the team on how this manifestation originated.

The Cu burrs signature was captured during the singulation stage of newly qualified quad-flat no-leads (QFN) product (hereinafter referred to as Device A) for critical customer. It was observed that burrs are out of specs and prone to shorting once reflowed at insert to the board at customer side. Device A defect parts per million (ppm) performance per assembly process given in Fig. 2 showed significant contribution of Cu burrs defect at singulation process. Actual ppm values are intentionally not shown due to confidentiality. Worthy to note that assembly process flow, in general, varies with the product and the technology [4-7].

2. EXPERIMENTAL SECTION

Potential causes of Cu burrs were itemized through fishbone analysis to cover all possible contributors. Trimming down the causes, why-why analysis was performed as holistic approach

to the problem. Succeeding discussions revealed the root-cause analysis and validations made for Cu burrs.

Digging deeper, further validation was made through why-why analysis as exemplified in Table 1. The leadframe design with full metal at saw lane was identified for causing the Cu burrs.

A dimensional analysis illustrated in Fig. 3 using computer-aided design (CAD) was performed to validate the original setup of the singulation tool.

The leadframe improvement was eventually implemented with the enhanced design of half-etched leads at the saw lane. An escape root-cause analysis shared in Table 2 was also done to reinforce robustness in the process and the solution.

For the escape root-cause, a corrective action was identified to explore the optimization of the vision system particularly the inspection program with respect to contrast.

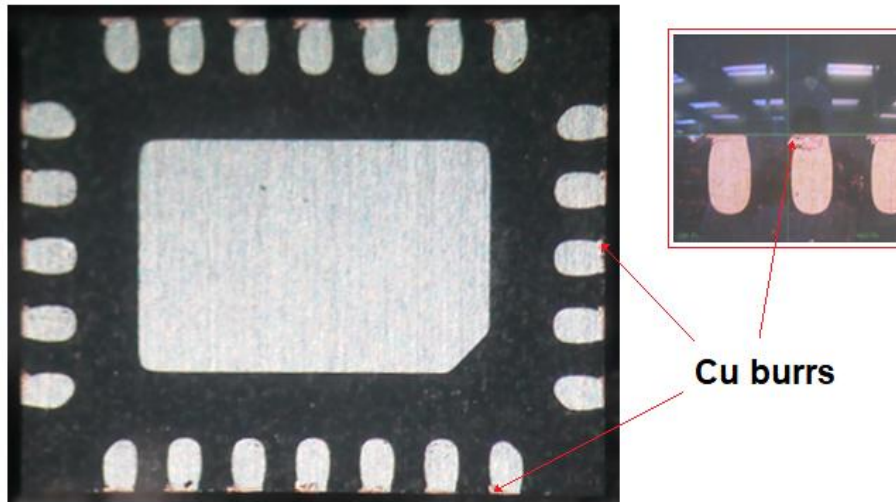


Fig. 1. Cu burrs defect manifestation

Table 1. Technical root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4
Out of specs copper burrs	Too much metal being cut	Leadframe design is full metal on saw lane	Wirebond requirement to address the stitch problem on 2 mil wire size

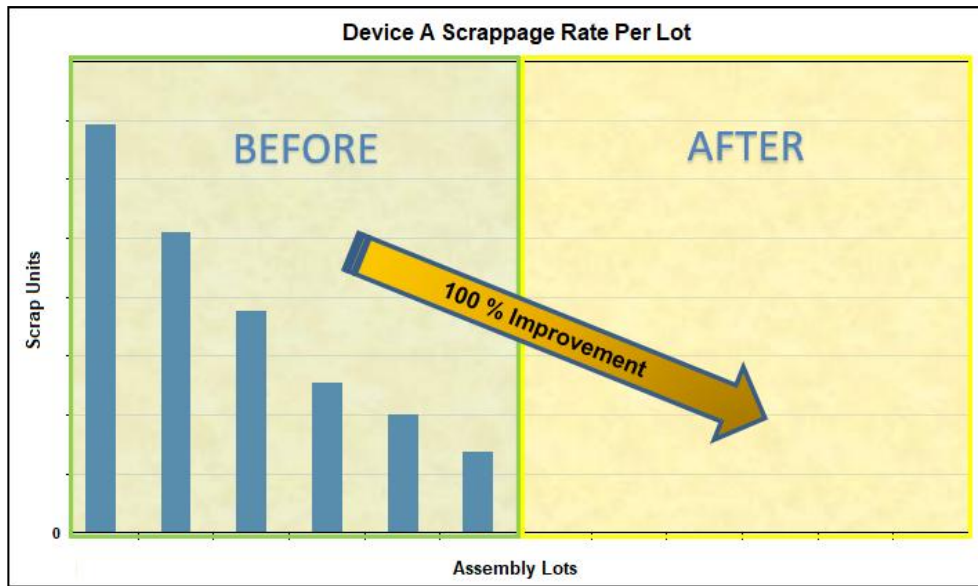


Fig. 4. Scrapage rate significant improvement

3. RESULTS AND ANALYSIS

Results of comprehensive investigation through fishbone and why-why analysis showed that the root-cause of Cu burrs is attributed to the leadframe design, specifically the full metal leads configuration at the saw lane. Results revealed that by using the enhanced leadframe design with half-etched metal leads at saw lane, Cu burrs occurrence was significantly mitigated as highlighted in the scrapage rate chart in Fig. 4. Actual values are intentionally not disclosed.

Significant effect was felt in the scrapage rate with 100 % improvement. Moreover, assembly yield trend stabilized after implementation of the enhanced leadframe design and all other corrective actions.

4. CONCLUSION AND RECOMMENDATIONS

The root-cause of the Cu burrs problem is attributed to the full metal design of the leadframe at singulation saw lane. After correction of leadframe design from full metal to half-etched leads at saw lane, Cu burrs occurrence was significantly eliminated.

It is recommended that the corrective actions be sustained by understanding the design coverage in the whole assembly process. This would help not to miss out all critical items when changes are made. Furthermore, the whole process

should undergo thorough review from technical team on the changes that will be implemented.

Although the paper focused on the improvement in the leadframe design to address the Cu burrs, continuous process and design improvement is imperative to sustain high quality performance of semiconductor products and its assembly manufacturing. Recommended future works could include studies on the effects and/or correlation of new and improved leadframe design on cutting method and speed optimization, the singulation blade life, and machine setup time improvement. Improvement in the visual inspection system could also be explored, as well as using deionized water to reduce heat during singulation and apply surfactant solution to mix with deionized water for smoother cutting. Also, discussions and works shared in [8-10] are useful in reinforcing robustness and optimization of package design and assembly processes. Moreover, it is equally important that the assembly manufacturing should observe proper electrostatic discharge (ESD) checks and controls. Discussions and learnings shared in [11-12] are helpful to comprehend proper and effective ESD-related controls.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely

no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
2. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
3. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008:1-11.
4. Nenni D, McLellan P. Fables: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
5. Harper C. Electronic packaging and interconnection handbook. 4th Ed., McGraw-Hill Education, USA; 2004.
6. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd Ed., CRC Press, USA; 2007.
7. Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA; 2016.
8. Sumagpang Jr. A, Gomez FR, Rodriguez R. Tool setup improvement for package scratch mitigation at end-of-line process. Journal of Engineering Research and Reports. 2020;12(3);1-5.
9. Rodriguez R, Gomez FR. Incorporating package grinding process for QFN thin device manufacturing. Journal of Engineering Research and Reports. 2020; 9(2);1-6.
10. Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
11. ESD Association. Fundamentals of ESD, device sensitivity and testing. USA; 2011.
12. Gomez FR, Mangaoang Jr. T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on qfn-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.

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